

# Solid-state memcapacitor

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We suggest a possible realization of a solid-state memory capacitive (memcapacitive) system. Our approach relies on the slow polarization rate of a medium between plates of a regular capacitor. To achieve this goal, we consider a multi-layer structure embedded in a capacitor. The multi-layer structure is formed by metallic layers separated by an insulator so that non-linear electronic transport (tunneling) between the layers can occur. The suggested memcapacitor shows hysteretic charge-voltage and capacitance-voltage curves, and both negative and diverging capacitance within certain ranges of the field. This proposal can be easily realized experimentally, and indicates the possibility of information storage in memcapacitive devices.

## I. INTRODUCTION

A recent experimental demonstration of a nanoscale memory-resistor (memristor for short)<sup>1</sup> has sparked numerous investigations in the area of materials and systems that show history-dependence in their current-voltage characteristics<sup>2-7</sup>. This has also led to the recent proposal and theoretical investigation of memcapacitors and meminductors, namely capacitors and inductors whose capacitance and inductance, respectively, depends on the past states through which the system has evolved<sup>8</sup>. Together with the memristor, the whole class of these memory-circuit elements promises new and unexplored functionalities in electronics, and the combination of these memory devices with their “standard” counterpart may find application in disparate areas of science and technology, including the study of neuromorphic circuits to simulate biological processes<sup>9</sup>. In this paper, we focus only on memcapacitors.

Various systems are known to exhibit memcapacitive behavior including vanadium dioxide metamaterials<sup>4</sup>, nanoscale capacitors with interface traps or embedded nanocrystals<sup>10-13</sup>, and elastic capacitors<sup>14,15</sup>. As anticipated in Ref. 8, memcapacitive effects may also accompany memristive effects in nanostructures, since in many of them the morphology of conducting regions changes in time<sup>1</sup>. Moreover, memcapacitors can be simulated by electronic circuits<sup>16</sup>. However, the number of experimentally identified memcapacitive systems is still very limited. In addition, it would be of great importance to identify a memcapacitive system that can be fabricated relatively easily, and is flexible enough to cover a wide range of capacitances.

Here, we suggest a possible realization of such a system based on the slow polarization of a medium between a regular capacitor plates. There are several physical mechanisms that can potentially provide a slowly polarizable medium. Examples include tunneling, activated drift of charged vacancies/impurities, slow ion penetration through a membrane, etc. In this paper, we will consider the tunneling mechanism and discuss a solid-

state memcapacitive system consisting of metal layers embedded into a parallel-plate capacitor as schematically shown in Fig. 1. In this realization, the internal metal layers, together with the insulator material, form a “metamaterial” characterized by a long polarization/depolarization time. The application of an external voltage to the capacitor leads to a charge redistribution between the embedded metal layers. The tunneling current between the layers depends almost exponentially on the applied voltage. This feature is important for the operation of our suggested device allowing for the “writing” of information (in the form of medium polarization) with high-voltage pulses, and “holding” such information when low/zero voltages are applied. The resulting memcapacitor exhibits not only hysteretic charge-voltage and capacitance-voltage curves but also both negative and diverging capacitance within certain ranges of the field. Due to its simplicity and unusual capacitance features we thus expect it to find use in both logic and memory applications.

This paper is organized as follows. Sec. II describes the theoretical framework used to simulate solid-state memcapacitors. Numerical simulations for the case of ac and

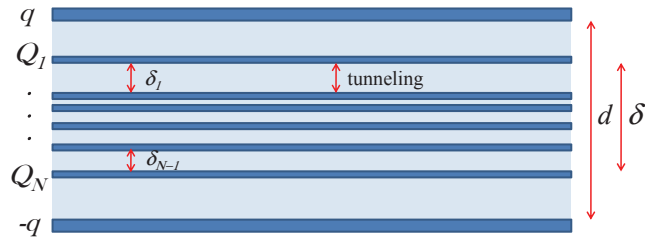


FIG. 1: General scheme of a solid-state memcapacitor. A metamaterial medium consisting of  $N$  metal layers embedded into an insulator is inserted between the plates of a “regular” capacitor. It is assumed that the electron transfer between external plates of the capacitor (with charge  $\pm q$ ) and internal metal layers (with charges  $Q_k$ ) is negligible. Therefore, the internal charges  $Q_k$  can only be redistributed between the internal layers creating a medium polarization.

pulsed applied voltages are presented in Sec. III and IV, respectively. An equivalent circuit model is given in Sec. V. Finally, Sec. VI presents our conclusions.

## II. MODEL

Quite generally, a circuit element with memory (memristor, memcapacitor or meminductor) is defined by the relations<sup>8</sup>

$$y(t) = g(x, u, t) u(t) \quad (1)$$

$$\dot{x} = f(x, u, t) \quad (2)$$

where  $u(t)$  and  $y(t)$  are any two input and output variables (i.e., current, charge, voltage, or flux),  $g$  is a generalized response,  $x$  is a set of  $n$  state variables describing the internal state of the system, and  $f$  is a continuous  $n$ -dimensional vector function. In this paper we will be concerned with only memcapacitors. Therefore, using Eqs. (1, 2), we define a charge-controlled memcapacitive system by the equations

$$V_C(t) = C^{-1}(x, q, t) q(t) \quad (3)$$

$$\dot{x} = f(x, q, t) \quad (4)$$

where  $q(t)$  is the charge on the capacitor at time  $t$ ,  $V_C(t)$  is the applied voltage, and  $C$  is the *memcapacitance*, which depends on the state of the system and can vary in time. Below, we identify the internal state variables of the solid-state memcapacitor shown in Fig. 1 and demonstrate that such memcapacitor is indeed described by Eqs. (3,4).

Let us then consider the system schematically shown in Fig. 1 consisting of  $N$  layers of metallic regions separated by an insulating material. This multi-layer system, of thickness  $\delta$ , is embedded into a standard parallel-plate capacitor. For convenience, although this is not necessary, we assume that the insulating material in between the embedded metallic layers is the same as the one of the regular capacitor. We also assume that our memcapacitor is designed in such a way that there is no electron exchange between the external plates and those embedded. This can be achieved by selecting an appropriate separation between the internal metal layers and the capacitor plates and/or by using an insulating material between the external capacitor plates and the embedded ones that generates a higher potential barrier. Therefore, in what follows, we assume that the tunneling only occurs between the internal metallic layers. Consequently, the total internal charge is always zero:  $\sum_{k=1}^N Q_k(t) = 0$ , where  $Q_k(t)$  is the charge on the internal metal layers at time  $t$ .

The operation of the polarization-based memcapacitor relies on the redistribution of the internal charges  $Q_k$  between the embedded layers caused by the electric field due to the charge  $q$  on the capacitor plates. Polarization

of the metamaterial results in an internal electric field between the layers that is opposite to the electric field due to the plate charges. Therefore, for a given amount of plate charge, the internal charges tend to decrease the plate voltage or, equivalently, to increase the capacitance.

Let us then calculate the internal charge distribution and consequent capacitance. A charged plane creates a uniform electric field in the direction perpendicular to the plane with a magnitude  $E = \sigma / (2\epsilon_0\epsilon_r)$ , where  $\sigma = q/S$  is the surface (of area  $S$ ) charge density,  $\epsilon_0$  is the vacuum permittivity, and  $\epsilon_r$  is the relative dielectric constant of the insulating material. Using this expression, we find that, in the structure shown in Fig. 1, the external plate voltage is given by,

$$V_C = 2dE_q + \delta E_1 + [\delta - 2\delta_1] E_2 + [\delta - 2(\delta_1 + \delta_2)] E_3 + \dots + [\delta - 2(\delta_1 + \dots + \delta_{k-1})] E_k \dots - \delta E_N, \quad (5)$$

where  $E_q = q/(2S\epsilon_0\epsilon_r)$  is the electric field due to the charge  $q$  at the external plate and  $E_k = Q_k/(2S\epsilon_0\epsilon_r)$  is the electric field due to the charge  $Q_k$  at the  $k$ -th embedded metal layer. Eq. (5) can also be written as follows

$$V_C = \frac{q}{C_0} \left[ 1 + \Delta \frac{Q_1}{2q} + (\Delta - 2\Delta_1) \frac{Q_2}{2q} + \dots + (\Delta - 2\Delta_{k-1}) \frac{Q_k}{2q} \dots - \Delta \frac{Q_N}{2q} \right], \quad (6)$$

where  $\Delta = \delta/d$ ,  $\Delta_i = \sum_{j=1}^i \delta_j/d$  for  $i = 1, 2, \dots, N-1$ ,  $\Delta_0 = 0$ , and  $C_0 = \epsilon_0\epsilon_r S/d$  is the capacitance of the system without internal metal layers. Therefore, the capacitance of the whole structure is

$$C = \frac{q}{V_C} = \frac{2C_0}{2 + \sum_{i=1}^N [\Delta - 2\Delta_{i-1}] \frac{Q_i}{q}}. \quad (7)$$

From this equation it is already clear that, unlike a conventional capacitor, there may be instants of time in which the denominator of Eq. (7) is zero while the numerator is finite. This may happen when the internal metal layers screen completely the external field, despite the presence of a finite charge  $q$  on the external capacitor plates. At these times one would then expect *diverging* values of capacitance. In addition, Eq. (7) does not enforce a positive capacitance. Indeed, as we will show in the examples below, at certain instants of time the internal metal layers may *over-screen* the external field, resulting in a *negative* capacitance. It is interesting to note that an hysteretic negative and diverging capacitance has been found also in ionic memcapacitors, namely nanopore membranes in an ionic solution subject to external time-dependent perturbations<sup>17</sup>. A negative capacitance has been experimentally observed in different solid-state systems<sup>18-20</sup>, but not accompanied by hysteretic and diverging values of capacitance.

In order to describe the dynamics of the internal charges  $Q_k$ , let us define  $V_k = -E_{k,k+1}\delta_k$  as the voltage between  $k$  and  $k+1$  metal layers. The electric field

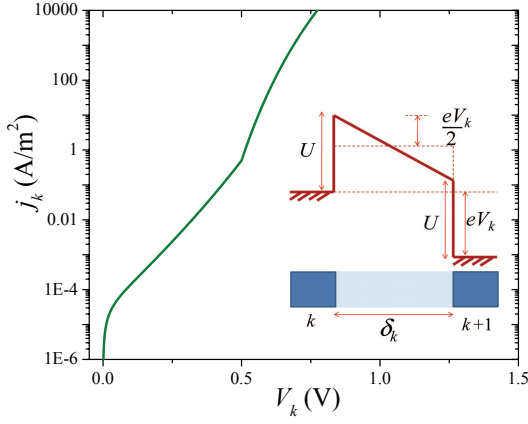


FIG. 2: Tunneling current density as a function of voltage drop between two adjacent internal layers calculated using the following values of parameters:  $U = 0.5\text{eV}$ ,  $\delta_k = 5\text{nm}$ , and  $m = m_e$ , with  $m_e$  the electron mass. Inset: the energy level scheme.

$E_{k,k+1}$  between two neighboring layers is obtained by adding the electric fields due to charges at all layers and at the external metal plates:

$$E_{k,k+1} = -2E_q - E_1 - E_2 \dots - E_k + E_{k+1} \dots + E_N = \frac{-2q - (Q_1 + \dots + Q_k) + (Q_{k+1} + \dots + Q_N)}{2S\epsilon_0\epsilon_r}. \quad (8)$$

The dynamics of the charge at a metal layer  $k$  is then determined by the currents flowing to and from that layer:

$$\frac{dQ_k}{dt} = I_{k-1,k} - I_{k,k+1}, \quad (9)$$

where  $I_{k,k+1}$  is the tunneling electron current flowing from layer  $k$  to layer  $k+1$  (note that for the top and bottom layers ( $k=1, N$ ), there is only one term on the right hand side of Eq. (9)). By considering the layer charges  $Q_k$  as state variables, we immediately notice that Eq. (9) is similar to Eq. (4). This demonstrates that the system under consideration is indeed a charge-controlled memcapacitive system.

If  $U$  is the potential barrier height between two adjacent metal layers (see inset of Fig. 2), the tunneling current induced by the voltage difference  $V_k$  between the two can be calculated using the following expressions<sup>21</sup>

$$I_{k,k+1} = \frac{Se}{2\pi h\delta_k^2} \left[ \left( U - \frac{eV_k}{2} \right) \exp \left[ -\frac{4\pi\delta_k\sqrt{2m}}{h} \sqrt{U - \frac{eV_k}{2}} \right] - \left( U + \frac{eV_k}{2} \right) \exp \left[ -\frac{4\pi\delta_k\sqrt{2m}}{h} \sqrt{U + \frac{eV_k}{2}} \right] \right] \quad (10)$$

if  $eV_k < U$ , and

$$I_{k,k+1} = \frac{Se^3 V_k^2}{4\pi h U \delta_k^2} \left[ \exp \left[ -\frac{4\pi\delta_k\sqrt{m}U^{3/2}}{ehV_k} \right] - \left( 1 + \frac{2eV_k}{U} \right) \exp \left[ -\frac{4\pi\delta_k\sqrt{m}U^{3/2}}{ehV_k} \sqrt{1 + \frac{2eV_k}{U}} \right] \right] \quad (11)$$

if  $eV_k > U$ . In the above equations,  $h$  is the Planck constant. The tunneling current density  $j_k = I_{k,k+1}/S$  as a function of voltage drop  $V_k$  is depicted in Fig. 2 for two adjacent layers. A strong increase in current with increase of  $V_k$  is clearly observed. This is an important property for the operation of our suggested memcapacitor.

### III. AC VOLTAGE OPERATION

In this Section, we present results of numerical simulations obtained for the case of a sinusoidal voltage  $V(t) = V_0 \sin(2\pi ft)$  of amplitude  $V_0$  and frequency  $f$  applied to a memcapacitor  $C$  connected in series with a resistor  $R$ . Such a circuit is described by the equation

$$V(t) = R \frac{dq}{dt} + \frac{q}{C}, \quad (12)$$

where, for  $C$ , we use Eq. (7). Eq. (12) is solved numerically together with Eq. (9) describing the internal charge dynamics. Below, we present results of numerical simulations for two different memcapacitor structures. In our simulations, a small value of  $R = 1\Omega$  is selected so that the voltage drop on the resistor is negligible.

#### A. 2-layer memcapacitor

The simplest system exhibiting polarization memory is a two-layer memcapacitor. In Fig. 3 we illustrate simulation results of such a device. Starting at the zero-charge state, the sinusoidal applied voltage induces electron tunneling between the internal metal layers resulting in non-zero  $Q_1$  and  $Q_2$ . As it is shown in Fig. 3(a), positive half-periods of  $V$  induce negative  $Q_1$  and positive  $Q_2$  charges. In turn, these cause a screening electric field opposite to the electric field of plate charges.

It is interesting that on the charge-voltage plot (Fig. 3(c)),  $q(V_C)$  forms a non-pinned hysteresis loop. This is a quite unusual feature of a memory device, especially, in view of the fact that, at the present time, only memristive devices exhibiting pinched hysteresis loops have been observed experimentally. Physically, it is clear that when an internal polarization in the memcapacitor is present and the plate charge is zero ( $q=0$ ), the internal polarization creates a non-zero voltage drop on the device  $V_C \neq 0$ . Alternatively, this voltage drop can be compensated by plate charges, but then we get  $V_C = 0$  at  $q \neq 0$ . This explains why the curve does not pass through the (0,0) point. The corresponding capacitance hysteresis is shown in Fig. 3(d). As expected, we find both negative and diverging capacitance values. In the vicinity of  $V_C = 0$ , the capacitance changes from  $+\infty$  to  $-\infty$  at

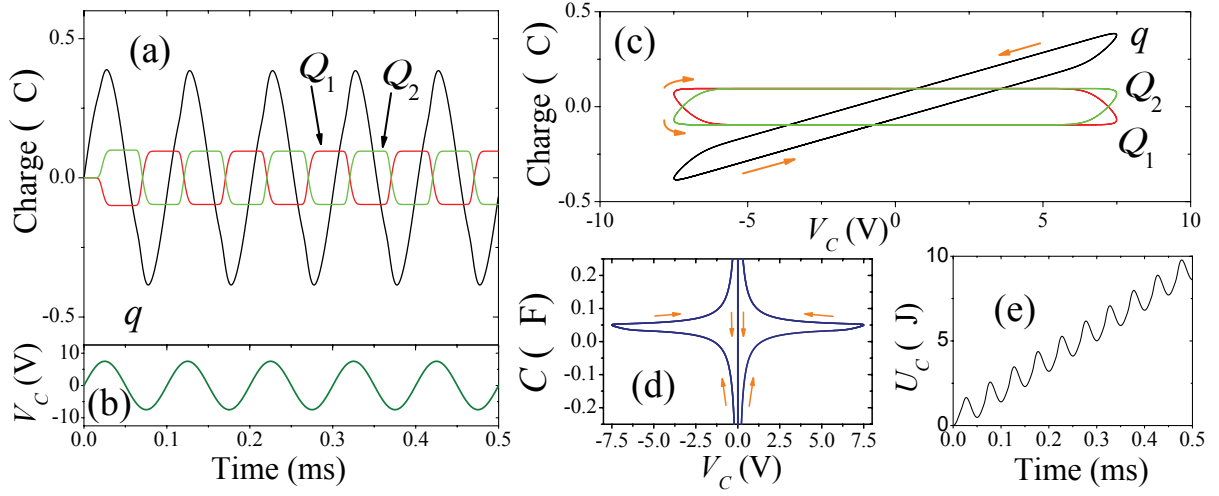


FIG. 3: Simulation of two-layer memcapacitor with symmetrically positioned internal layers. (a) The charge on internal metallic layers and memcapacitor plates as a function of time  $t$ . (b) Voltage on memcapacitor,  $V_C$ , as a function of time  $t$ . Charge-voltage (c) and capacitance-voltage (d) plots. (e) Added/removed energy as a function of time  $t$ . These plots were obtained using the parameter values  $V_0 = 7.5\text{V}$ ,  $f = 10\text{kHz}$ ,  $d = 100\text{nm}$ ,  $\delta = 66.6\text{nm}$ ,  $S = 10^{-4}\text{m}^2$ ,  $\epsilon_r = 5$ ,  $U = 0.33\text{eV}$ ,  $R = 1\Omega$ .

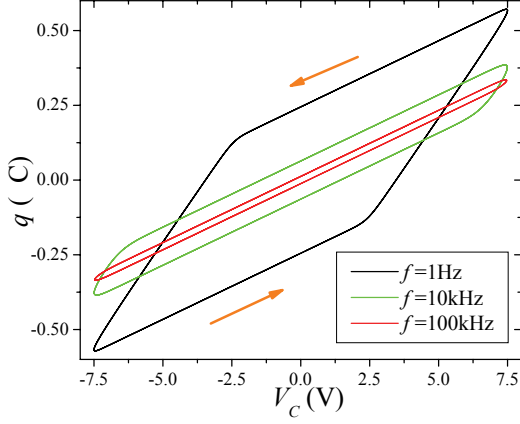


FIG. 4: Charge-voltage plot at different applied voltage frequencies  $f$ . The decrease of the hysteresis at higher frequencies is a signature of memcapacitors<sup>8</sup>. The calculation and device parameters are as in Fig. 3.

both sweep directions. In Fig 3(d), these abrupt changes appear as two coinciding vertical lines.

Next, we consider the added/removed energy to/from the capacitor which is defined as

$$U_C = \int_0^t V_C(\tau) I(\tau) d\tau. \quad (13)$$

From Fig. 3(e) it is clear that the present solid-state memcapacitor operates as a dissipative device since the amount of added energy is on average larger than the amount of removed energy (resulting in positive values of  $U_C$  at all times). This occurs because the electron tunneling between internal layers is accompanied by energy dissipated in thermalization processes due to the

different electrochemical potential energies of metal layers. In addition, in a real device we cannot exclude the phenomenon of local heating that would also contribute to dissipation of energy<sup>22</sup>.

In fact, the energy dissipation in electron transfer processes or the usual energy dissipation in dielectric materials described by the imaginary part of the complex permittivity can be used as an alternative to our approach. The heat released can drive a phase transition in a material between the plates, such as transition from crystalline to amorphous state and vice versa, accompanied by a change in material's permittivity. In this way, the memcapacitor acquires a long-term memory based directly on the value of  $\epsilon_r$ . The required material for this purpose can be similar to chalcogenide glass, which can be "switched" between two states, crystalline or amorphous, with the application of heat, but possibly at a lower phase transition temperature. The device operation protocol can then be based in applications of ac-modulated voltage pulses whose amplitude, duration or frequency can control the material's state.

Finally, the frequency behavior of the charge-voltage hysteresis loop is shown in Fig. 4. It is clearly seen that the hysteresis shrinks at higher frequencies. This is a typical behavior of memory devices<sup>8</sup> related to the fact that at high frequencies the internal degrees of freedom of a memory device do not have enough time to respond to the external perturbation. Similarly, with increasing frequency, we have observed a decrease in capacitance hysteresis as well as in the rate of energy dissipation.

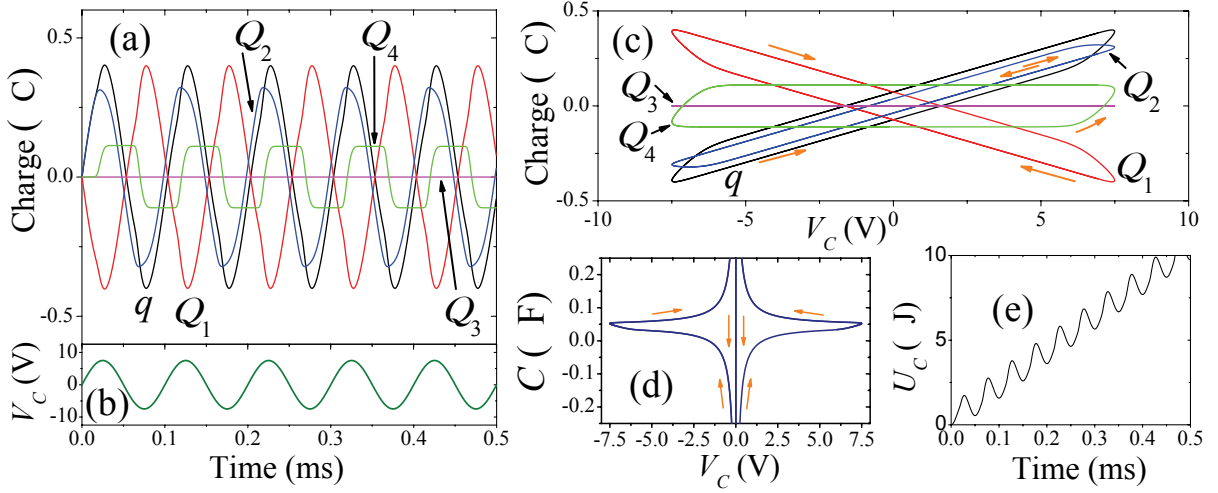


FIG. 5: Simulation of four-layer memcapacitor. (a) The charge on internal layers and memcapacitor plates as a function of time  $t$ . (b) Voltage on memcapacitor  $V_C$  as a function of time  $t$ . Charge-voltage (c) and capacitance-voltage (d) plots. (e) Added/removed energy as a function of time  $t$ . These plots were obtained using the same parameter values as in Fig. 3. The locations of internal layers are defined by parameters  $\delta_1 = 0.024\delta$ ,  $\delta_2 = \delta_3 = 0.488\delta$ .

### B. Multi-layer memcapacitor

The results obtained for multi-layer memcapacitors are similar to the two-layer memcapacitor case. The only interesting difference is that in the case of multi-layer memcapacitors, a richer internal charge dynamics can be observed. Charge dynamics is essentially determined by the distance between the layers and the potential energy barrier between adjacent layers. As a prototype of multi-layer memcapacitor, we consider a four-layer memcapacitor.

In our particular example two additional internal layers (2-nd and 3-rd) were inserted between the two layers of the two-layer memcapacitor. The layers' positions are specified in the caption of Fig. 5: layer 2 is positioned close to layer 1, while layer 3 is placed in between layers 2 and 4. As a result, the electron tunneling current can be high between 1-st and 2-nd layers which is reflected in high amplitudes of  $Q_1$  and  $Q_2$ . Concerning the charge on the third layer, it is essentially close to zero. We explain it by a tendency of maximum charge separation in these types of devices. Fig. 5 displays our simulation results for this case. One can also see that the capacitance hysteresis and the added/removed energy (Fig. 5 (d) and (e), respectively) are similar to those of the two-layer memcapacitor as shown in Fig. 3.

## IV. RETRIEVING THE MEMCAPACITOR STATE

At this point, an important question is how one can read the memcapacitor state. Here, we demonstrate that the most simple way to do it is by using a single voltage pulse. Small amplitude or short voltage pulses are not

suitable for this purpose as they do not change the charge distribution on the internal layers considerably. Therefore, the measured value of capacitance, using small amplitude or short pulses, would always be equal to  $C_0$ , the capacitance in the absence of the internal metal layers. It is thus important to ensure that the applied pulse has a large enough amplitude and is sufficiently long. Consequently, the device state will be altered by the pulse. However, since the initial state is read by this measurement, this state can be, in principle, restored.

Fig. 6 illustrates the reading of the internal layer polarization in a two-layer memcapacitor. Quite generally, we start with a memcapacitor having a certain internal polarization and assume that at the initial moment of time the voltage drop on the memcapacitor is zero. Although this is not a steady state of the device (at  $t \rightarrow \infty$  and  $V_C = 0$  we expect  $q, Q_k \rightarrow 0$ ), the memcapacitor can stay in such a state sufficiently long since the tunneling current is exponentially suppressed at low internal fields. Our idea is to apply a single voltage pulse to the device and monitor the amount of charge needed to make  $V_C$  close to the applied voltage  $V$ . This amount of charge  $\Delta q$ , as we show, depends on the device state.

In our particular calculations, we consider two cases characterized by a different initial polarization. When  $Q_1$  is negative at  $t = 0$  (Fig. 6(a)), the applied voltage pulse does not significantly change the device state ( $Q_1, Q_2$ ) and the amount of charge  $\Delta q$  added to the plates is small (hence the capacitance is low). In the opposite case, when  $Q_1$  is positive at  $t = 0$  (Fig. 6(b)), much larger charge should be transferred to the capacitor plates since “re-programming” of the internal state is required. Therefore, this measurement would monitor a higher value of capacitance. We emphasize that the measured capacitance value is determined by both the



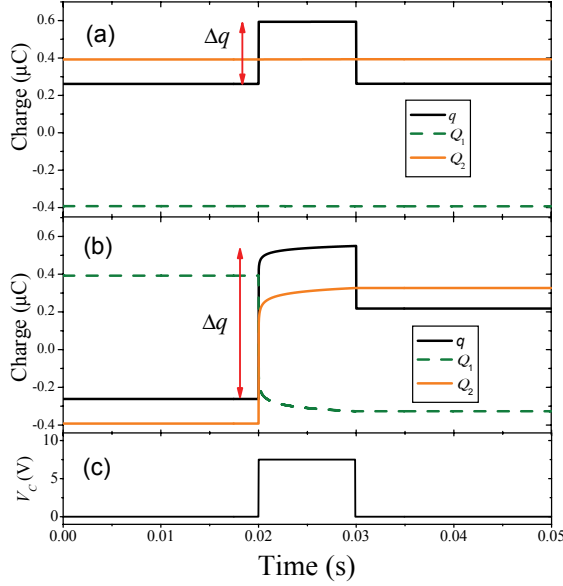


FIG. 6: The amount of charge  $\Delta q$  needed for the same change in  $V_C$  (by 7.5V in the present calculation) depends on the initial memcapacitor polarization. (a) and (b) represent the device dynamics at different initial conditions, while (c) is the voltage pulse profile. The memcapacitor parameters are as in Fig. 3.

system state and by the voltage probe. For the same system state but different probes (for example, pulses of different polarity but of same magnitude) the measured value of capacitance may be different.

## V. EQUIVALENT CIRCUIT MODEL

In this Section, we suggest an equivalent circuit model of the solid-state memcapacitor discussed above. This correspondence is very useful in circuit simulators, or in the realization of electronic circuits to reproduce memcapacitive features. The main idea behind the circuit model is to represent each insulator spacing between adjacent metal layers (including capacitor plates) by a separate capacitor and to use non-linear resistors in order to mimic the electron tunneling between the layers and energy loss in the thermalization processes accompanying the tunneling. The top and bottom surfaces of each internal layer are considered as plates of adjacent circuit model's capacitors while the metallic material of the layer itself plays the role of the conductor connecting these capacitors.

Fig. 7(a) shows the equivalent circuit of a two-layer memcapacitor. The circuit is composed by three capacitors connected in series. The capacitor in the middle is connected in parallel to a non-linear resistor (see Fig. 7(a)). The parameters of capacitors are determined by the usual parallel plate capacitor expression and related

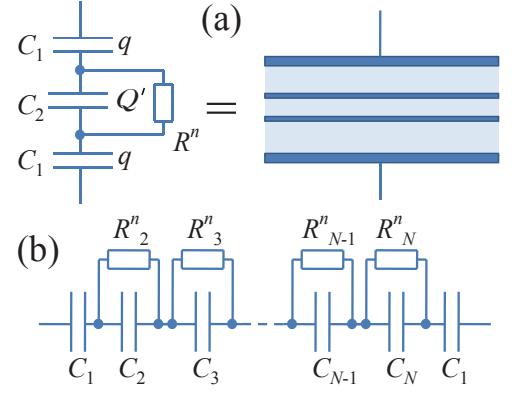


FIG. 7: (a) Equivalent circuit model of two-layer memcapacitor. Here,  $C_1$  and  $C_2$  are usual capacitors and  $R^n$  is a non-linear resistor. It is assumed that the internal layers are symmetrically embedded into the device. Otherwise, the capacitance values of all capacitors would be different. (b) Equivalent circuit model of  $N$ -layer memcapacitor.

to the parameters of memcapacitor in the following way:

$$C_1 = \frac{\varepsilon_0 \varepsilon_r S}{(d - \delta)/2} = \frac{2C_0}{1 - \Delta},$$

$$C_2 = \frac{\varepsilon_0 \varepsilon_r S}{\delta} = \frac{C_0}{\Delta}.$$

Next, we demonstrate the equivalence of the equations describing the circuit model and those of the memcapacitor. The circuit shown in Fig. 7(a) is described by the following two equations

$$V_C = \frac{2q}{C_1} + \frac{Q'}{C_2} \quad (14)$$

$$\frac{dq}{dt} = \frac{dQ'}{dt} + I_R, \quad (15)$$

where the first equation is for the total voltage drop and the second equation is the Kirchhoff's law for the currents. Here,  $I_R$  stands for the current through the non-linear resistor which depends on the voltage drop on  $C_2$  (equal to  $Q'/C_2$  with  $Q'$  the charge on capacitor  $C_2$ ).

Solving Eqs. (14,15) for the total capacitance we obtain

$$C = \frac{q}{V_C} = \frac{C_1 C_2}{2C_2 + C_1 \frac{Q'}{q}} = \frac{C_0}{1 + \Delta \frac{Q' - q}{q}}, \quad (16)$$

$$\frac{d(Q' - q)}{dt} = -I_R. \quad (17)$$

In order to relate Eqs. (16,17) to the memcapacitor equations from Sec. II, we note that the sum of charges at the bottom plate of  $C_1$  (equal to  $-q$ ) and at the top plate of  $C_2$  (equal to  $Q'$ , see Fig. 7(a)) is equal to  $Q_1$ , that is the charge at the first layer of memcapacitor, i.e.,  $Q_1 = Q' - q$ . One then immediately notices that Eq. (16) and Eq. (7) (for the case of two layers) are exactly the same; Eq. (17) and Eq. (9) are also the same. This

proofs the complete equivalence between memcapacitor's and circuit model's equations.

The extension of the circuit model to an  $N$ -layer memcapacitor is straightforward:  $N - 1$  different capacitors and non-linear resistors must be introduced between the external capacitors  $C_1$ . Fig. 7(b) shows the equivalent circuit model of an  $N$ -layer memcapacitor. Another interesting model extension can be achieved if a memristive dielectric material (e.g.,  $\text{VO}_2$  films<sup>5</sup>) is used instead of the usual dielectric in the device. Then, in the equivalent circuit model, the role of non-linear resistors will be played by memristors.

## VI. CONCLUSION

In conclusion, we have suggested and analyzed a solid-state memcapacitor made of a multi-layer structure embedded in a capacitor. The resulting system has noteworthy features, such a frequency-dependent hysteresis under an ac-voltage, diverging and negative capacitance. These features emerge due to the slow polarizability of the internal multi-layer structure as a consequence of electron tunneling between the internal metal layers. This gives rise to both complete screening of the field due to the external metal plates - giving rise to diverging capacitances - and over-screening of the same field leading to negative capacitances. Clearly, when combined to an external circuit with finite capacitance, the capacitance divergencies of our proposed solid-state capacitor would be cut off by the external circuit. Nonetheless, both the information

stored in this memcapacitor in a continuous fashion (analog operation) and its negative capacitance in a certain range of the external field, may find useful applications in electronics. In particular, we have suggested a simple way to read the information stored in the capacitor by using appropriate single pulses.

We have also shown the equivalent circuit model for this memcapacitor based on a combination of regular capacitors and non-linear resistors. This analogy could be useful both in actual calculations with circuit simulators, or in experiments with electronic circuits to reproduce memcapacitive features. Finally, it is worth stressing that the memcapacitor presented in this work can be easily fabricated by growing a metamaterial of several metallic layers separated by an insulator (e.g., an oxide) in between the metallic plates of a regular capacitor. Since only "standard" materials (as opposed to ferroelectrics) are used, the suggested memcapacitor should also show high reliability. Several modifications of the suggested structure are possible, such as suggested in the text use of phase change or memristive materials as well as e.g. use of nano-size metal beads instead of metal layers. We thus hope this work will motivate experimental research in this direction.

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